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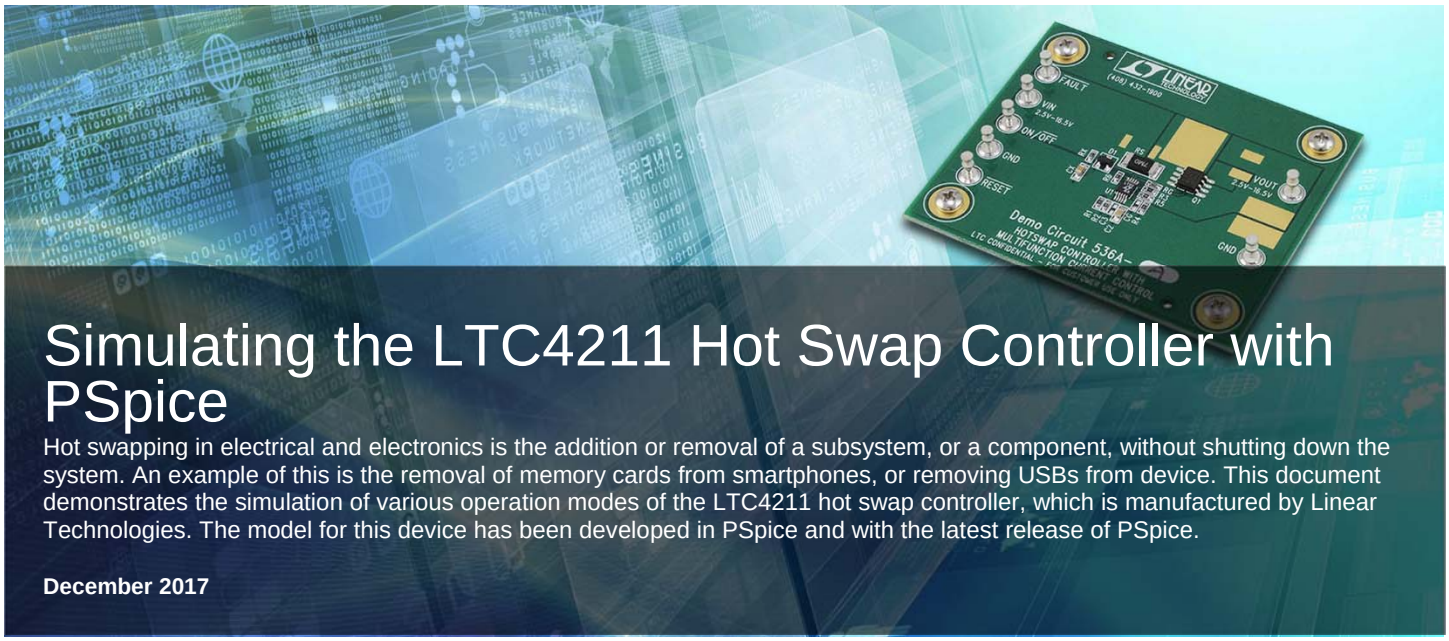

Simulating the LTC4211 Hot Swap Controller with PSpice

Hot swapping in electrical and electronics is the addition or removal of a subsystem, or a component, without shutting down the system. An example of this is the removal of memory cards from smartphones, or removing USBs from device. This document demonstrates the simulation of various operation modes of the LTC4211 hot swap controller, which is manufactured by Linear Technologies. The model for this device has been developed in PSpice and with the latest release of PSpice.

December 2017

Overview

This application note has:

- A brief overview of the various device operating modes
- The location of the model
- A design example
- Application circuits for various operating modes
    - Startup operation
    - Circuit-breaker operation
    - Overcurrent operation
    - PCB connection sense

About the Device

LTC4211 is available in two package versions, MS8 (8-pin) and MS (10-pin). It is a hot swap controller that enables a PCB board to be safely inserted or removed from a live backplane, or system. When PCBs are inserted into, or removed from, live systems, the supply bypass capacitors can draw huge transient currents from the backplane power bus while charging. These transient current glitches, or surges, can damage the connector pins as well as cause other boards in the system to malfunction. LTC4211 is designed to turn the printed circuit board's supply voltages ON and OFF, in a controlled manner with internal supervision, allowing a subsystem to be removed or inserted, without any malfunction.

Where to Find This Model

The symbol for this part is available in the *SPECIAL_PURPOSE_ICS* library at the following location:
`INSTALLATION>\TOOLS\CAPTURE\LIBRARY\PSPICE\SPECIAL_PURPOSE_ICS`

OrCAD Capture and PSpice Design Example

Startup Operation

Figure 1 shows a typical hot swap controller application circuit diagram for LTC4211.

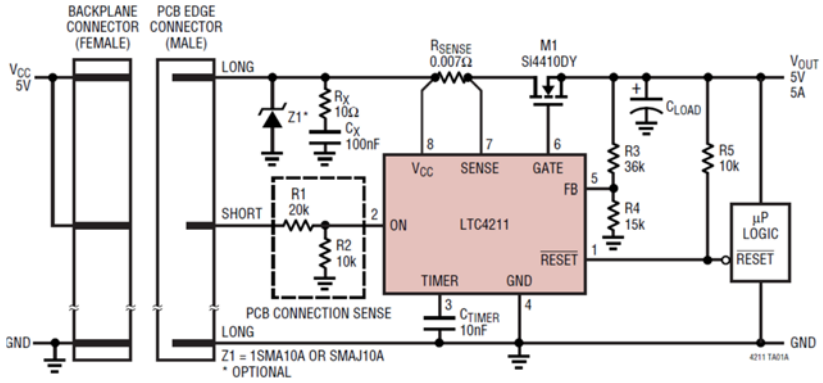

Figure 1 Hot swap controller application circuit diagram

Figure 2 shows the application circuit schematic for Figure 1.

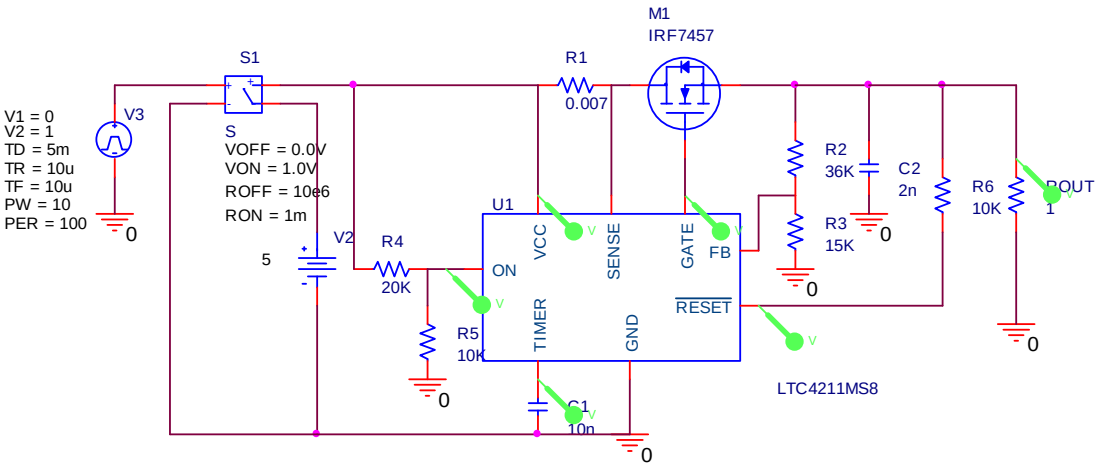

Figure 2: Application circuit schematic

Select the *5V_hot_swaping* schematic, and select the *5V_hot_swaping-tran* as the active simulation profile.

Referring to Figure 3, when a PCB board is first inserted into a live backplane, a startup check is done to ensure the supply voltage is above its 2.3 V UVLO threshold (see Time Point 1), here the insertion of PCB is depicted by switch S1 and VPULSE V3, which starts the device after 5 mS. Once VCC and ON are valid (ON pin valid means voltage at ON pin is greater than1.316), LTC4211 checks if the GATE is OFF (VGATE < 0.2V) at Time Point 2. An internal timing circuit is enabled and the TIMER pin voltage ramps up as per the capacitor attached to the TIMER pin. At Time Point 3 (the timing period programmed by C1 capacitor), the TIMER pin voltage equals VTMR (1.236V). Next, the TIMER pin voltage ramps down to Time Point 5 where fast comparator is armed.

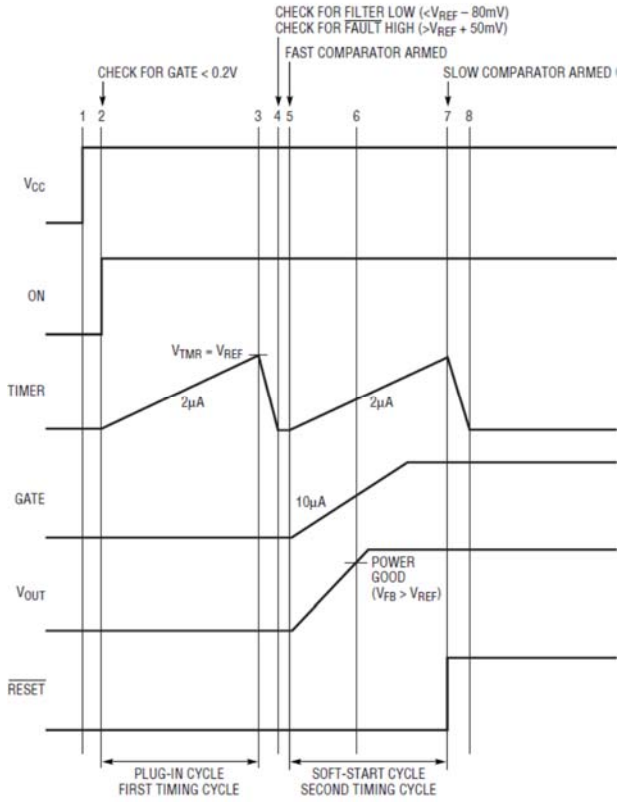

Figure 3 Normal power up sequence as defined in datasheet

In LTC4211 MS, the following two additional checks are done:

1. FILTER pin voltage is low (VFILTER < 1.156V)
2. FAULT pin voltage is high (VFAULT > 1.286V) are done at Time Point 4

If the above conditions are met, LTC4211 begins a second timing (soft-start) cycle, at the peak of which slow comparator is armed.

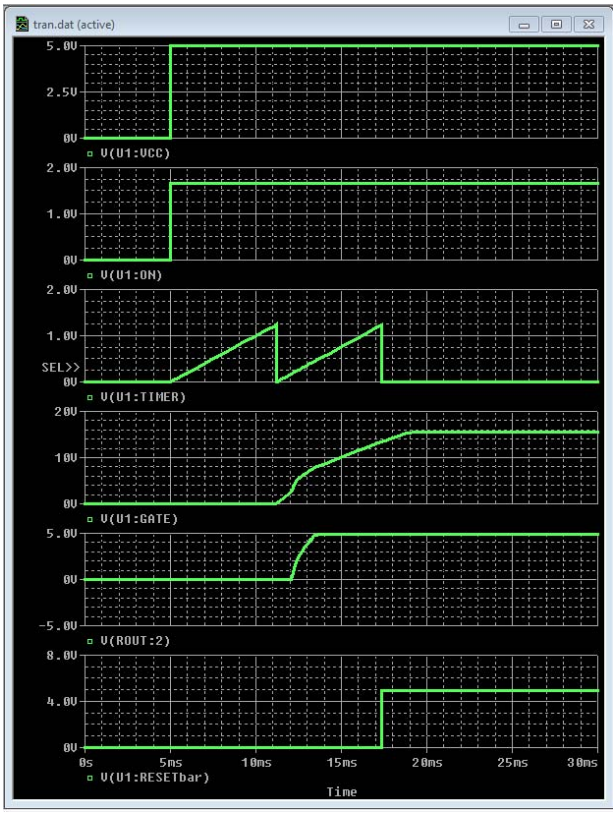

Figure 4 Power up sequence as obtained in simulation

The timer capacitor charging up rate is:

$$C_{TIMER}\ \text{Charge-Up Rate} = \frac{2\mu A}{C_{TIMER}}$$

LTC4211 automatically limits the inrush current by controlling the GATE pin voltage slew rate. During the second timing cycle, if the inrush is large enough to cause a voltage drop greater than 50mV across the sense resistor, the device senses this, and controls the current source at the GATE pin to regulate the load current to:

$$I_{LIMIT(SOFTSTART)} = \frac{50mV}{R_{SENSE}}$$

LTC4211 features an electronic circuit breaker function that protects against supply overvoltage, externally generated fault conditions, shorts, and excessive load current conditions on the supply. If the circuit breaker trips, the GATE pin is instantly grounded, and the voltage at FAULT is latched low and the device is turned off. The circuit breaker usually has some buffer time before tripping and grounding the gate pin voltage. If the fault condition is cleared within this duration, the device is not turned off and operates normally. This duration is defined by the SLOW and FAST comparators, which are triggered depending on the voltage across the RSENSE resistors.

To adjust the response time of SLOW COMP, the MS version of LTC4211 is chosen, and a capacitor is used at the LTC4211's FILTER pin, otherwise it is fixed to 20 us. The FAST COMP trips the circuit breaker to protect against fast load over currents if the transient voltage across the sense resistor is greater than 150 mV for 300 ns. The response time of LTC4211 FAST COMP is fixed for both 8 and 10 pin version.
To clear the internal fault, detect circuitry and to restart the LTC4211, its ON pin must be driven low (VON < 1.236V) for at least 150 us, after which the time FAULT goes high. Toggling the ON pin from low to high (VON > 1.316V) initiates a restart sequence in the LTC4211.

Overcurrent operation

Select the overcurrent schematic and set overcurrent-Tran as the active simulation profile.

Now let's see how can we simulate these conditions in PSpice. In the circuit diagram shown in Figure 5, we have created a circuit to simulate over current condition. In this example, the goal is to simulate dead short condition at output. This is achieved by connecting a controlled circuit (V5 and S1) directly connected across the load. The fault is triggered at 8 ms during the second timing cycle. Now as per the device datasheet, the device should go into current limit mode and the current through MOSFET (M1) should be reduced to maintain a 50 mv voltage drop across RSENSE for the duration of the time cycle, which is till 13 msec. If this fault persists even after second timing cycle, the slow comparator triggers the circuit breaker operation. In this testbench, the slow comparator will trip the circuit breaker as the voltage drop across the sense resistor > 50mv for a duration greater than 638 us (approximately) after the end of second timing cycle. Now, the voltage at FAULT pin is pulled Low. The device is in OFF state.

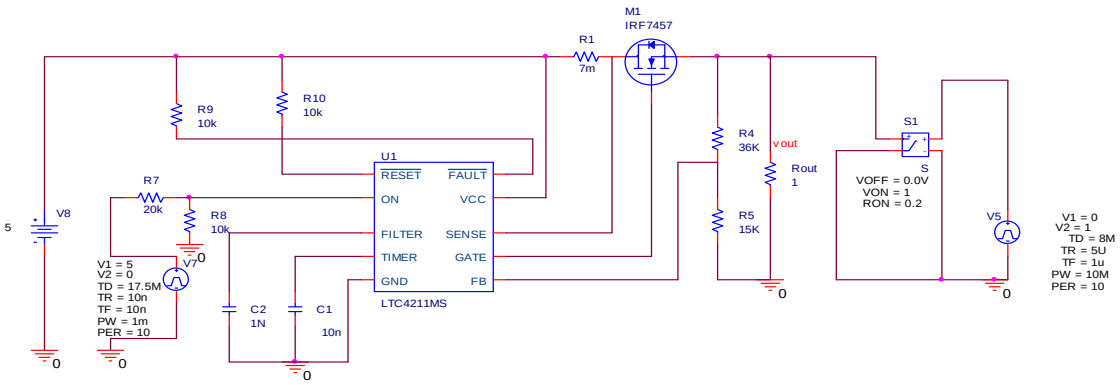

Figure 5 Circuit for overcurrent mode of operation

To restart the device, the voltage at ON pin is cycled from low to high for duration > 150 us. this is done by Pulse Source V7 at 17.5 ms. The fault condition is cleared at 17.654 ms. The device restarts at 18.503 ms once the voltage at ON pin is high again.

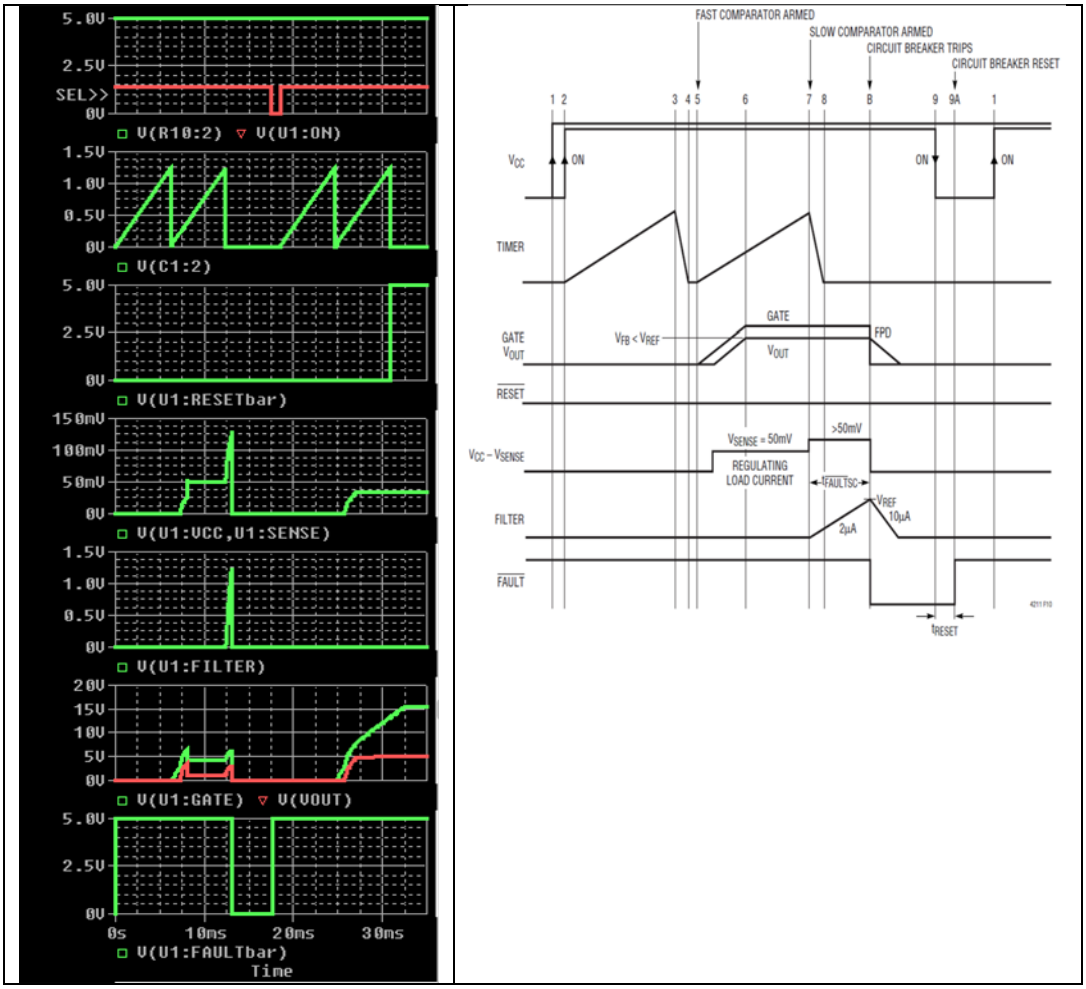

Figure 6 Simulation results for overcurrent mode

Circuit breaker operation

We will now simulate both the slow and fast comparator circuit breaker operations.

Select the *cricuit_breaker* schematic and set *cricuit_breaker-Tran* as the active simulation profile.

Referring to Figure 7, the slow comparator trips (VSENSE > 50 mv) after 368 us from 20 ms. This is achieved in the circuit by using Vpulse source V8, which is configured to provide a surge of overvoltage (>50mv) across RSENSE resistor R7 and the device is shutdown.

Using Vpulse V7, the ON pin voltage is cycled low to high at 25 ms with duration > 150 us, to restart the device at 26 ms.
Similarly, using switch S1 and Vpulse Source V5, dead short condition at output is created. Fast comparator trips when voltage across RSENSE resistor R7 > 150mv for more than 300 ns. Here this condition is asserted at 50.0009093 ms and the device shuts at 150 ns after this.

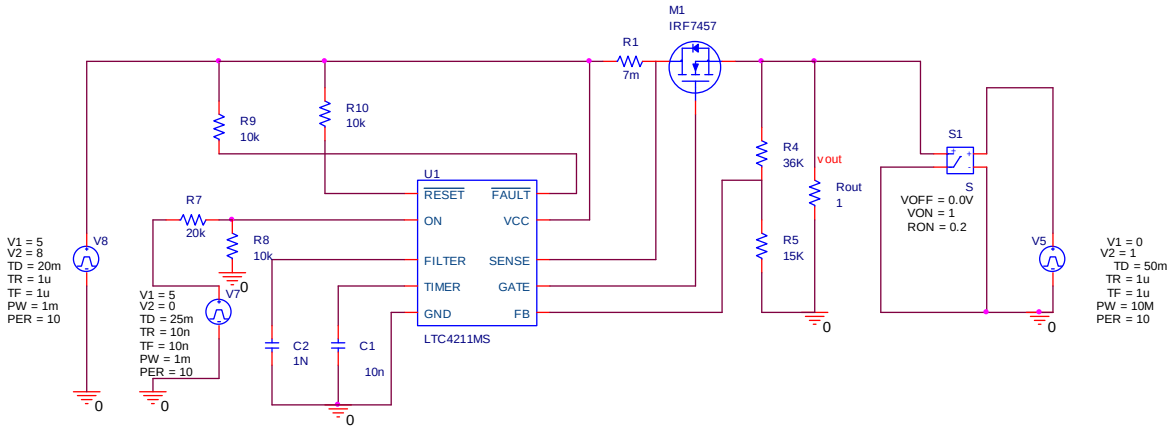

Figure 7 Circuit diagram for circuit breaker operation

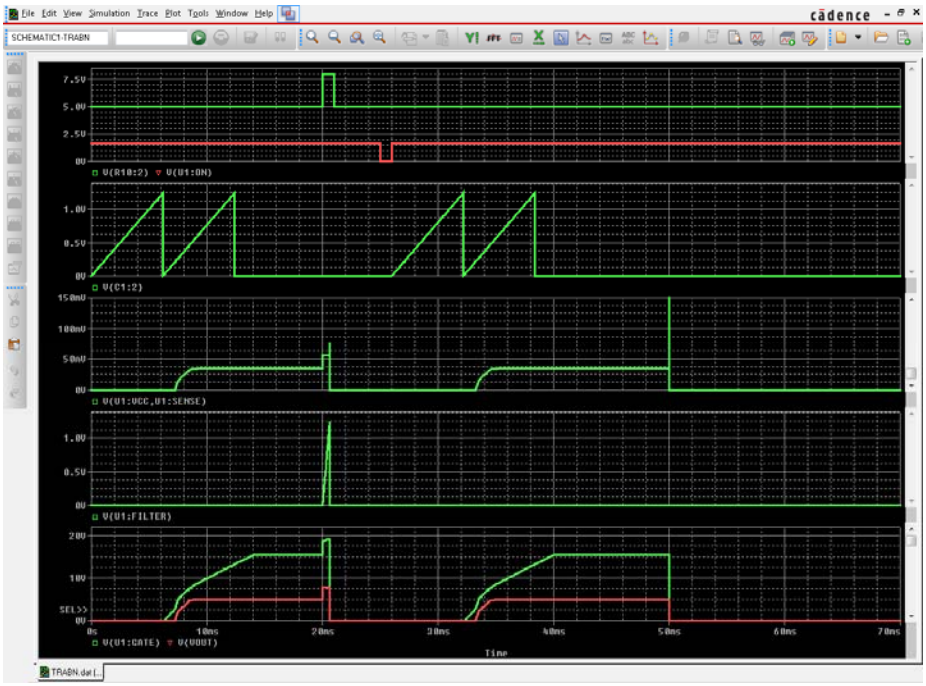

Figure 8 Simulation result for circuit breaker operation

PCB connection sense

It is to detect whether the printed circuit board has been fully seated in the backplane before the LTC4211 commences a start-up cycle.
Figure 9 connection sense with on off control

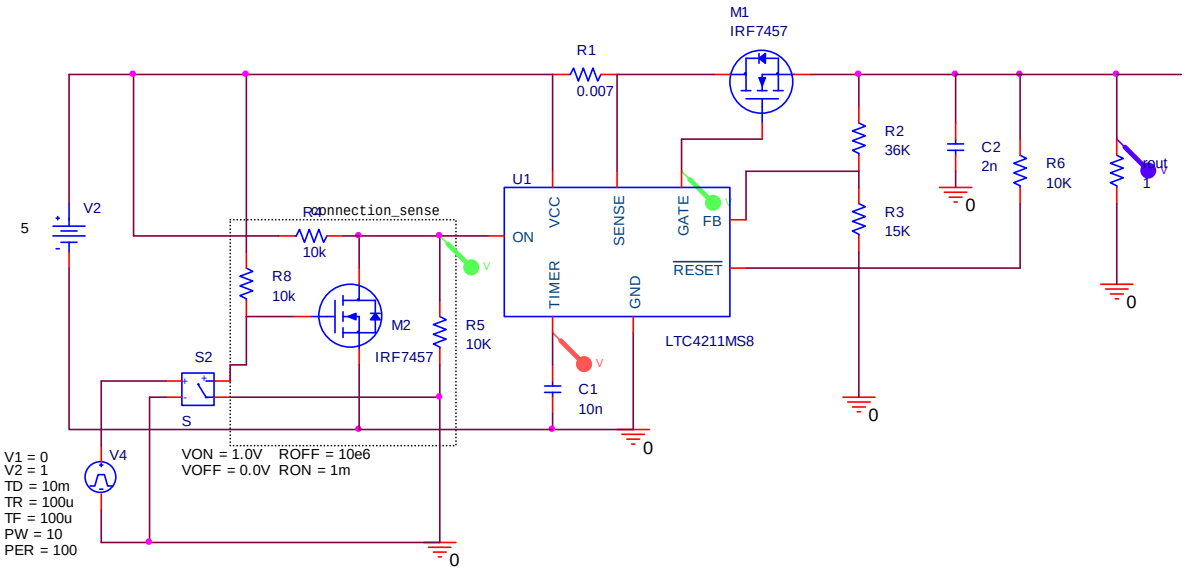

Figure 9 Circuit diagram for connection sense with on off control

Here the switch S2 and vpulse V4 act as backplane connecters and allow startup only after gate of M2 is grounded. A MOSFET and resistors combination offers processor interrupt control . R8 keeps the gate of M2 at VCC until the system is perfectly connected to the backplane. A logic low to the gate turns M2 OFF, allows the ON pin to pull high and turns on LTC4211.

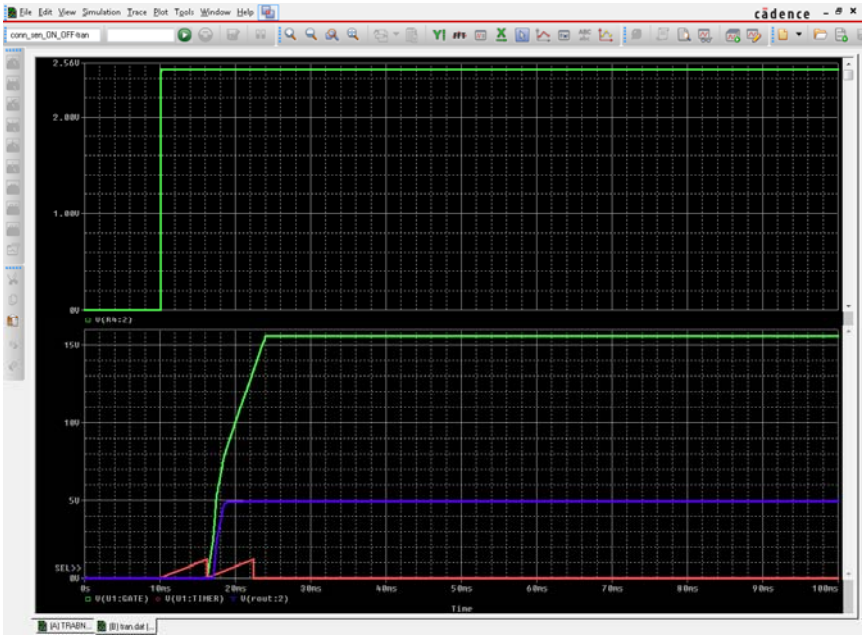

Figure 10 Simulation results for connection sense with on off control

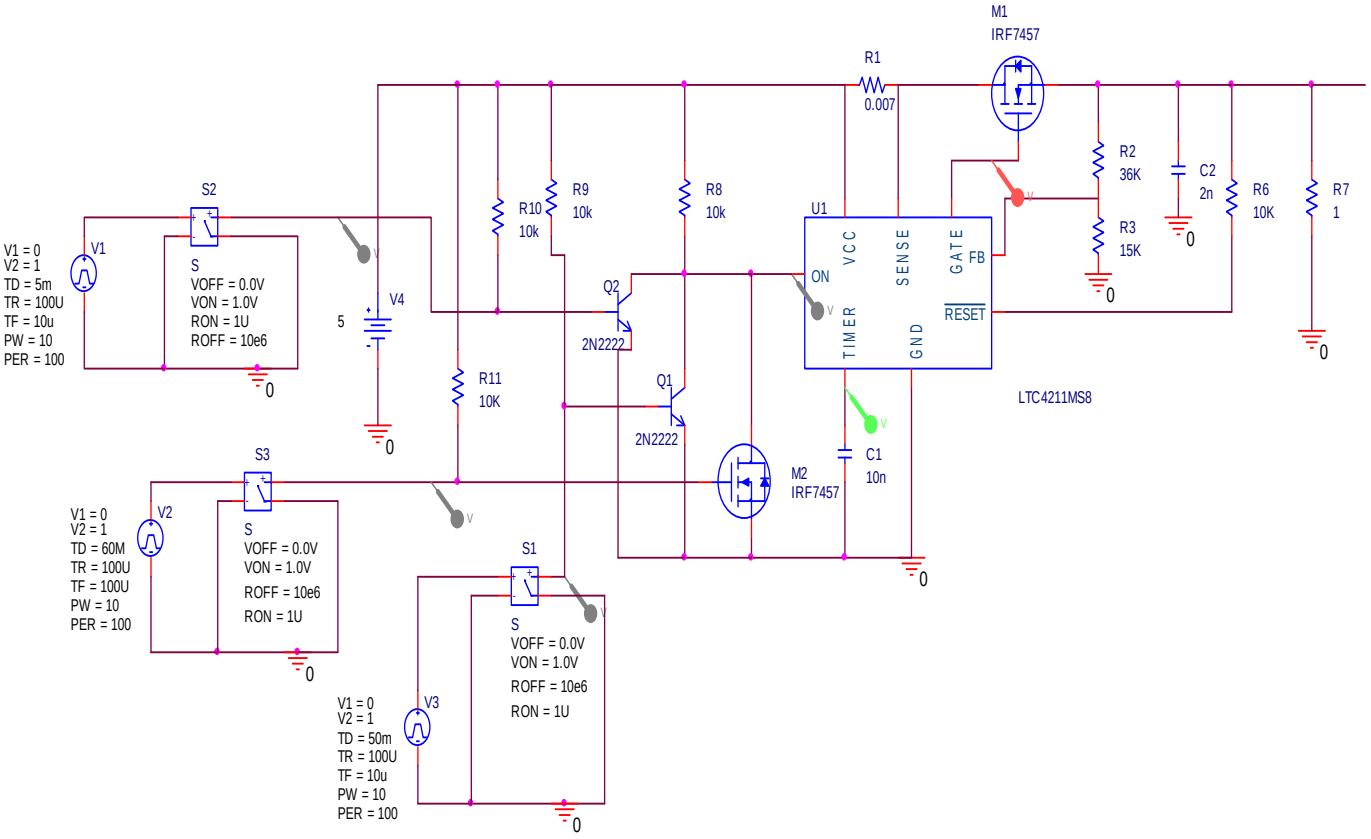

Figure 11 Circuit diagram for connection sense for rocking the PCB back and forth

The installation or removal of printed circuit cards generally requires rocking the card back and forth. The switches S1, S2, and S3 act shot length wire as shown in the next figure.

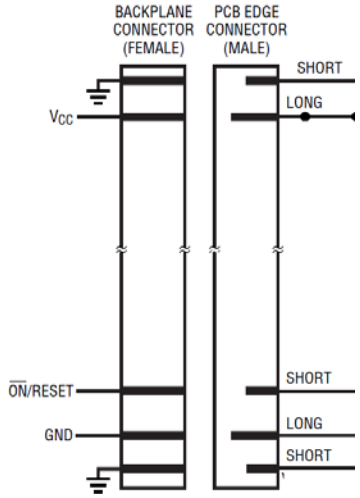

Figure 12 Diagram of backplane and PCB edge connector

Along with MOSFET, when VCC makes connection, the bases of transistors Q1 and Q2 are pulled high, turning them ON. The LTC4211 model is in OFF state when either of Q1 or Q2 are ON state, since These tranisitor Keep the 'ON' Pin grounded. When the base and gate connector pins of M2, Q1, and Q2 are connected to the backplane, they are grounded, turning them OFF. The 'ON' pin voltage is then pulled high by R8 turning LTC4211 Model ON

Referring to Figure 11, LTC4211 starts only after the gate and bases of MOSFET M2 and transistors Q1 and Q2 are grounded, that is after 60 ms.

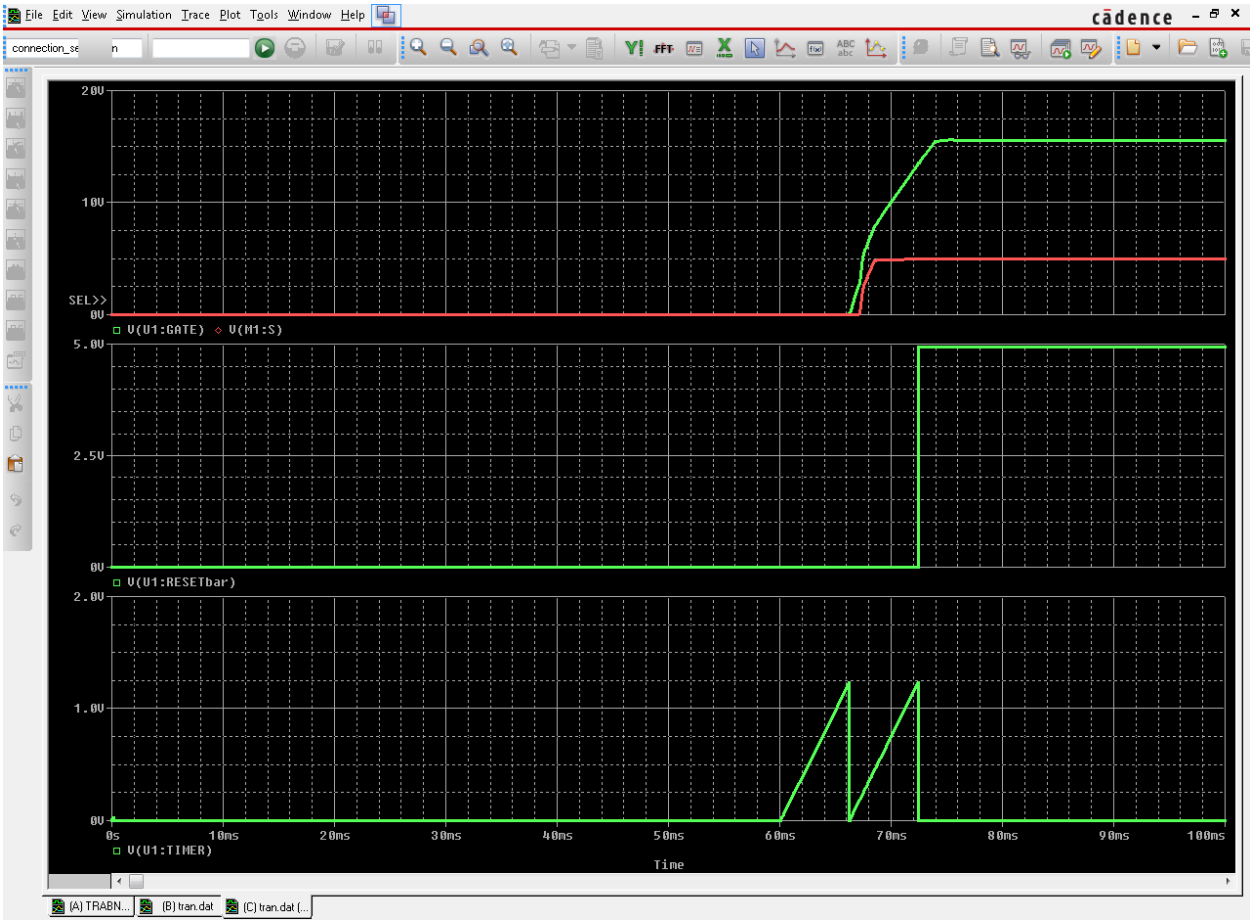

Figure 13 Simulation results for connection sense for rocking the PCB back and forth

Limitations of the Model Implemented in PSpice

The following known limitations exist at this time:

- Glitch filter time is constant with respect to feedback transient voltage
- Some of the typical electrical characteristic values in the datasheet might not match the model
- The temperature effects are not modeled

References

This document is based on the LTC4211 datasheet.